CLAIMS

What is claimed is:

1. A method of fabricating a memory device with a recessed channel comprising:

selectively etching trenches in a semiconductor substrate;

forming an oxide layer within at least the trenches;

depositing a first conductive layer over the semiconductor substrate and in the trenches;

planarizing the device to selectively remove portions of the first conductive layer while leaving portions of the first conductive layer in the trenches to form gates;

performing one or more bitline implants to form bitlines adjacent to the gates;

removing portions of the oxide layer located in the trenches adjacent to the polysilicon gates to a first depth defining gap regions;

partially filling the gap regions with a lower insulating layer;

depositing a charge trapping material within at least the gap regions on the lower insulating layer; and

forming an upper insulating layer on the deposited charge trapping material.

2. The method of claim 1, wherein the deposited first conductive layer is comprised of polysilicon.

3. The method of claim 1, wherein removing portions of the oxide layer comprises performing a wet etch process to remove the portions.

4. The method of claim 1, wherein the deposited lower insulating layer is comprised of oxide and the deposited upper insulating layer is comprised of oxide.

5. The method of claim 1, wherein the charge trapping material deposited is nitride.

6. The method of claim 1, further comprising:

selectively etching the device to expose an upper surface of the gates; and

forming a second conductive layer on the device, wherein the second conductive layer is in contact with the gates.

7. The method of claim 6, further comprising forming a third insulating layer over the second conductive layer and planarizing the third insulating layer.

8. The method of claim 7, further comprising etching trenches through the third insulating layer to the bitlines and forming at least partially aligned contacts therein.

9. The method of claim 1, wherein the deposited first conductive layer is doped polysilicon.

10. The method of claim 1, wherein the charge trapping material is nitride and is deposited *via* a low pressure chemical vapor deposition process.

11. The method of claim 1, wherein the charge trapping material is deposited by depositing a lower portion of the charge trapping material in the gap region, depositing an insulating material in the gap region forming a charge gap, and depositing an upper portion of the charge trapping material.

12. The method of claim 1, wherein the lower insulating layer is also deposited over the bit line regions and the charge trapping layer is also formed on the lower insulating layer over the bitline regions.

13. A method of fabricating a memory device with a recessed channel comprising:

selectively etching trenches in a semiconductor substrate;

forming an insulating layer within at least the trenches;

depositing a first conductive layer over the semiconductor substrate and in the trenches;

selectively removing portions of the first conductive layer while leaving portions of the first conductive layer in the trenches to form gates;

performing one or more bitline implants to form bitlines adjacent to the gates;

removing portions of the insulating layer located in the trenches adjacent to the polysilicon gates to a first depth defining gap regions;

partially filling the gap regions with an insulating material;

removing the insulating material from the gap regions and an additional amount of the insulating layer remaining in the trenches to expand the gap regions to a second depth that is greater than the first depth;

forming a lower insulating layer in at least the gap regions;

depositing a charge trapping material within at least the gap regions on the lower insulating layer; and

forming an upper insulating layer on the deposited charge trapping material.

14. The method of claim 13, wherein the charge trapping material is nitride.

15. The method of claim 13, wherein the insulating material is oxide.

16. A method of fabricating a memory device with a recessed channel comprising:

forming shallow trench isolation regions in a semiconductor substrate within a periphery region of the device;

selectively etching core trenches in a semiconductor substrate within a core region of the device;

forming an insulating layer within at least the core trenches;

depositing a first conductive layer over the semiconductor substrate and in the trenches;

selectively removing portions of the first conductive layer while leaving portions of the first conductive layer in the trenches to form gates within the core region;

performing a bitline implant to form bitlines within the core region adjacent to the gates;

selectively forming well regions within the periphery region;

removing portions of the insulating layer located in the trenches adjacent to the gates to a first depth defining gap regions;

partially filling the gap regions with a lower insulating layer;

depositing a charge trapping material within at least the gap regions on the lower insulating layer; and

forming an upper insulating layer on the deposited charge trapping material.

17. The method of claim 16, further comprising selectively etching portions of the second conductive layer within the periphery region to form gate structures within the periphery region.

18. The method of claim 17, wherein the second conductive layer is doped polysilicon.

19. A U-shaped memory device comprising:

first and second bitline regions formed within a semiconductor substrate;

a partially recessed gate formed within the semiconductor substrate in between the first and second bitline regions;

a U-shaped channel region that extends below the gate between the first and second bitline regions; and

a first and second charge trapping region located adjacted to sidewalls of the polysilicon gate and the first and second bitline regions.

20. The device of claim 19, wherein the first and second charge trapping regions are comprised of a lower oxide, nitride, and an upper oxide.

21. The device of claim 19, wherein an oxide-nitride-oxide layer is formed over the first and second bitline regions.

22. The device of claim 19, further comprising a wordline formed over the first and second bitlines and on the gate.

23. The device of claim 19, wherein the first and second charge trapping regions include a vertical segment of nitride.

24. The device of claim 23, wherein the vertical segment of nitride includes a gap comprised of oxide.